

That Which is Claimed is:

1. Electronic memory circuit comprising a matrix of EEPROM memory cells, each incorporating:
 - a MOS floating gate transistor (2a) and
 - a selection transistor (5),the matrix of the type comprising a plurality of rows (3) and columns (4), each row (3) being provided with a word line (WL) and each column (4) comprising a bit line (BL) organized in line groups so as to group said matrix cells in bytes (9a), each of which has a control gate line (CG) associated, characterized in that
 - a pair of cells (2) having a common source region (6), each cell (2) being arranged symmetrically with respect to said common source region (6), has a common control gate region (12).
2. Electronic circuit according to claim 1, characterized in that
 - the pairs of cells (2), having the source region (6) in common, belong to the same byte (9a).
3. Electronic circuit according to claim 2, characterized in that the common control gate regions (12) of the pairs of cells belonging to the same byte are connected to the same control gate line (CG).
4. Electronic circuit according to claim 3, characterized in that an enabling transistor (T) addresses the common control gate line.
5. Electronic circuit according to claim 4, characterized in that said enabling transistor (T) is a MOS transistor.

6. Electronic circuit according to claim 1, characterized in that the common control gate region (12) covers the common source region (6).

7. Process for manufacturing an electronic memory circuit, comprising a matrix of EEPROM memory cells. comprising the steps of:

- formation of active areas;
- 5 - implantation of strongly doped regions (9);
- formation of layers (10, 13) of oxide of different thickness;
- implantation of a common source region (6);
- 10 - selective deposition of a first layer (14) of polysilicon;
- selective removal of said first layer from the common source region (6);
- deposition of an intermediate dielectric layer;
- 15 - deposition of a second layer (17) of polysilicon;
- realization of only one control gate region (12) for pairs of cells having the source region (6) in common.

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